

DATA SHEET

TDA1554Q

**4 x 11 W single-ended or 2 x 22 W
power amplifier**

Product specification
File under Integrated Circuits, IC01

May 1992

4 x 11 W single-ended or 2 x 22 W power amplifier

TDA1554Q

GENERAL DESCRIPTION

The TDA1554Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs ($V_P = 0$ V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μ A
Stereo BTL application						
Output power	$R_L = 4 \Omega$; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	$R_S = 0 \Omega$	$V_{no(rms)}$	–	70	–	μ V
Input impedance		$ Z_i $	25	30	38	k Ω
DC output offset voltage		$ \Delta V_o $	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	$R_L = 4 \Omega$	P_o	–	6	–	W
	$R_L = 2 \Omega$	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	$R_S = 0 \Omega$	$V_{no(rms)}$	–	50	–	μ V
Input impedance		$ Z_i $	50	60	75	k Ω

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243R); SOT243-1; 1996 July 23.

4 x 11 W single-ended or 2 x 22 W power amplifier

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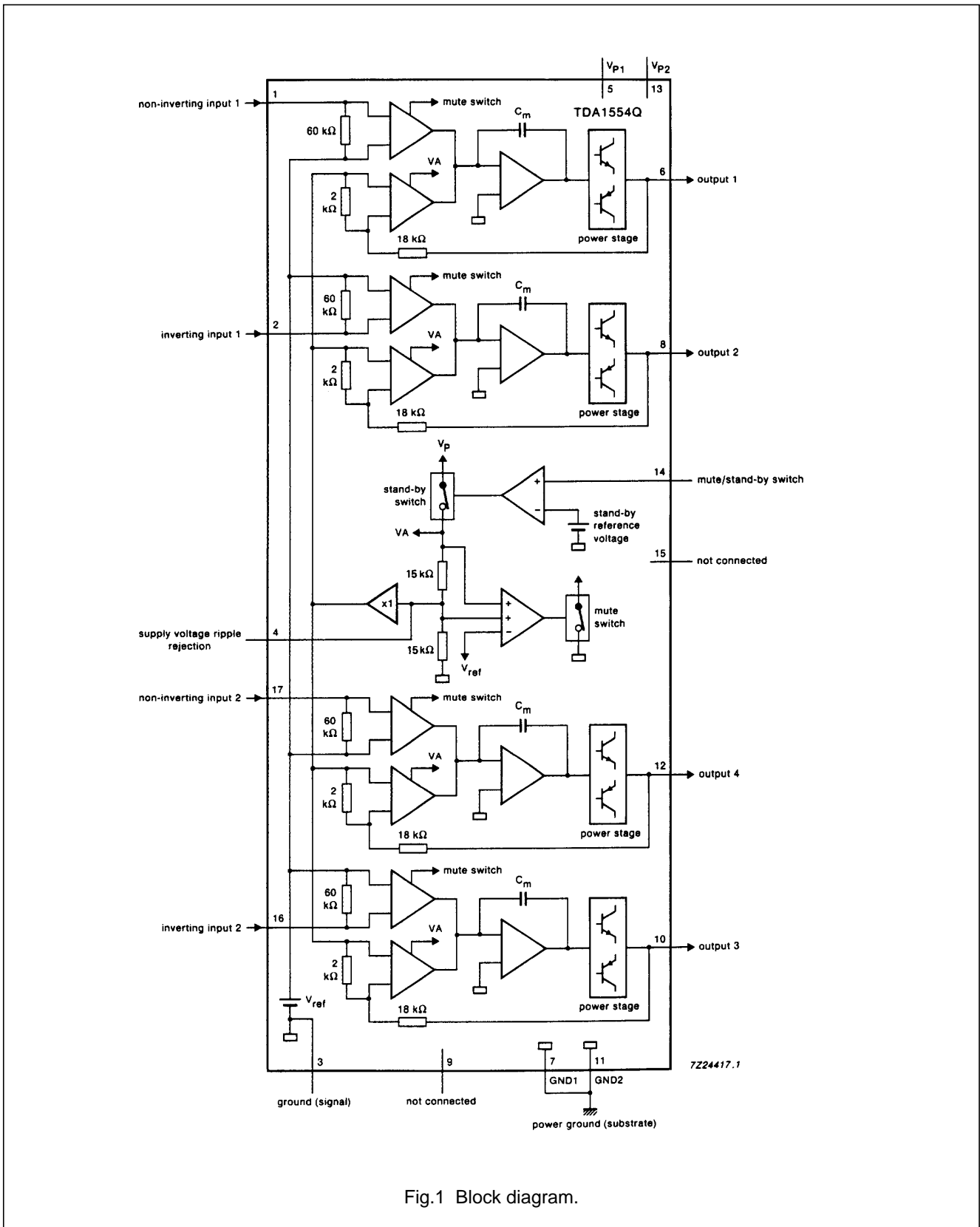


Fig.1 Block diagram.

4 x 11 W single-ended or 2 x 22 W power amplifier

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PINNING

1	NINV1	non-inverting input 1	9	n.c.	not connected
2	INV1	inverting input 1	10	OUT3	output 3
3	GND	ground (signal)	11	GND2	power ground 2 (substrate)
4	RR	supply voltage ripple rejection	12	OUT4	output 4
5	V _{P1}	positive supply voltage 1	13	V _{P2}	positive supply voltage 2
6	OUT1	output 1	14	M/SS	mute/stand-by switch
7	GND1	power ground 1 (substrate)	15	n.c.	not connected
8	OUT2	output 2	16	INV2	inverting input 2
			17	NINV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1554Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). A special feature of this device is:

Mute/stand-by switch

- low stand-by current (< 100 μ A)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage					
operating		V _P	–	18	V
non-operating		V _P	–	30	V
load dump protected	during 50 ms; t _r ≥ 2.5 ms	V _P	–	45	V
Non-repetitive peak output current		I _{OSM}	–	6	A
Repetitive peak output current		I _{ORM}	–	4	A
Storage temperature range		T _{stg}	–55	+ 150	°C
Junction temperature		T _j	–	150	°C
AC and DC short-circuit-safe voltage		V _{PSC}	–	18	V
Energy handling capability at outputs	V _P = 0 V		–	200	mJ
Reverse polarity		V _{PR}	–	6	V
Total power dissipation	see Fig.2	P _{tot}	–	60	W

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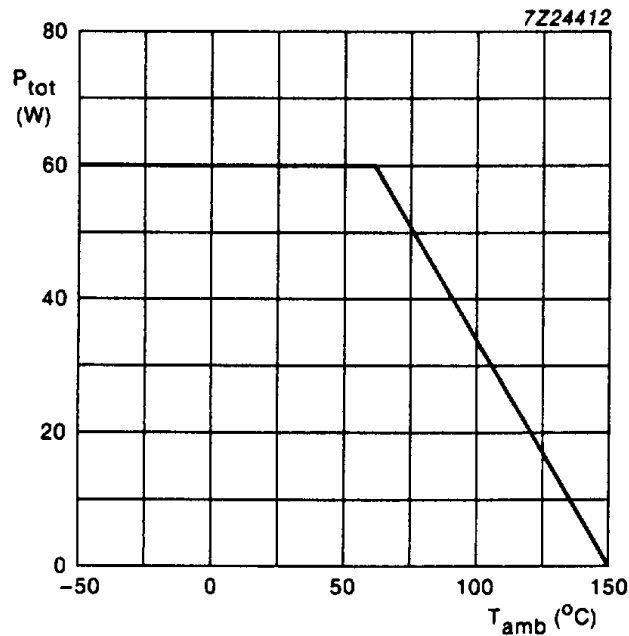


Fig.2 Power derating curve.

DC CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; measurements taken using Fig.4; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$ \Delta V_O $	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	$V_I = 1$ V (max); $f = 1$ kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$ \Delta V_O $	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μ A
Switch-on current		I_{sw}	–	12	40	μ A

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AC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; $T_{amb} = 25\text{ °C}$; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at $V_P = 13.2\text{ V}$	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	$P_o = 1\text{ W}$	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%					
	$P_o = -1\text{ dB}$ w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3					
	-1 dB	f_L	–	45	–	Hz
High frequency roll-off	-1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$ Z_{i} $	25	30	38	k Ω
Noise output voltage (RMS value)						
ON	$R_S = 0\ \Omega$; note 5	$V_{no(rms)}$	–	70	–	μV
ON	$R_S = 10\text{ k}\Omega$; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	$R_S = 10\text{ k}\Omega$	α	40	–	–	dB
Channel unbalance		$ \Delta G_v $	–	–	1	dB

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at $R_L = 2\ \Omega$	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	$P_o = 1\ \text{W}$	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	–3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_V	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$ Z_i $	50	60	75	$k\Omega$
Noise output voltage (RMS value)						
ON	$R_S = 0\ \Omega$; note 5	$V_{no(rms)}$	–	50	–	μV
ON	$R_S = 10\ k\Omega$; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	$R_S = 10\ k\Omega$	α	40	–	–	dB
Channel unbalance		$ \Delta G_V $	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at $V_P = 6\ \text{V}$ to $18\ \text{V}$ and AC operating at $V_P = 8.5\ \text{V}$ to $18\ \text{V}$.
2. At $18\ \text{V} < V_P < 30\ \text{V}$ the DC output voltage $\leq V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of $0\ \Omega$ (maximum ripple amplitude of $2\ \text{V}$) and a frequency between $100\ \text{Hz}$ and $10\ \text{kHz}$.
5. Noise voltage measured in a bandwidth of $20\ \text{Hz}$ to $20\ \text{kHz}$.
6. Noise output voltage independent of R_S ($V_I = 0\ \text{V}$).
7. Output power is measured directly at the output pins of the IC.

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APPLICATION INFORMATION

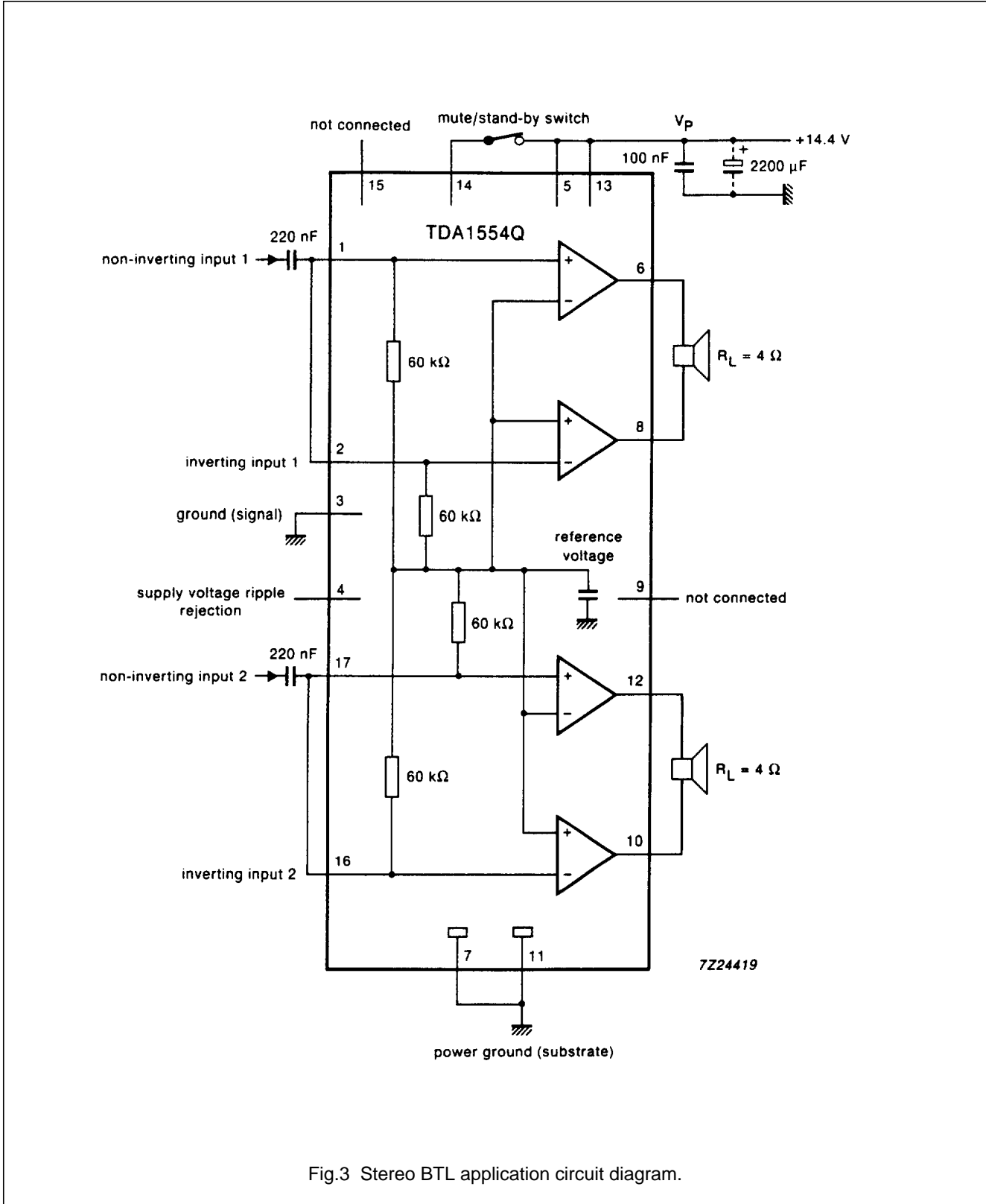


Fig.3 Stereo BTL application circuit diagram.

4 x 11 W single-ended or 2 x 22 W power amplifier

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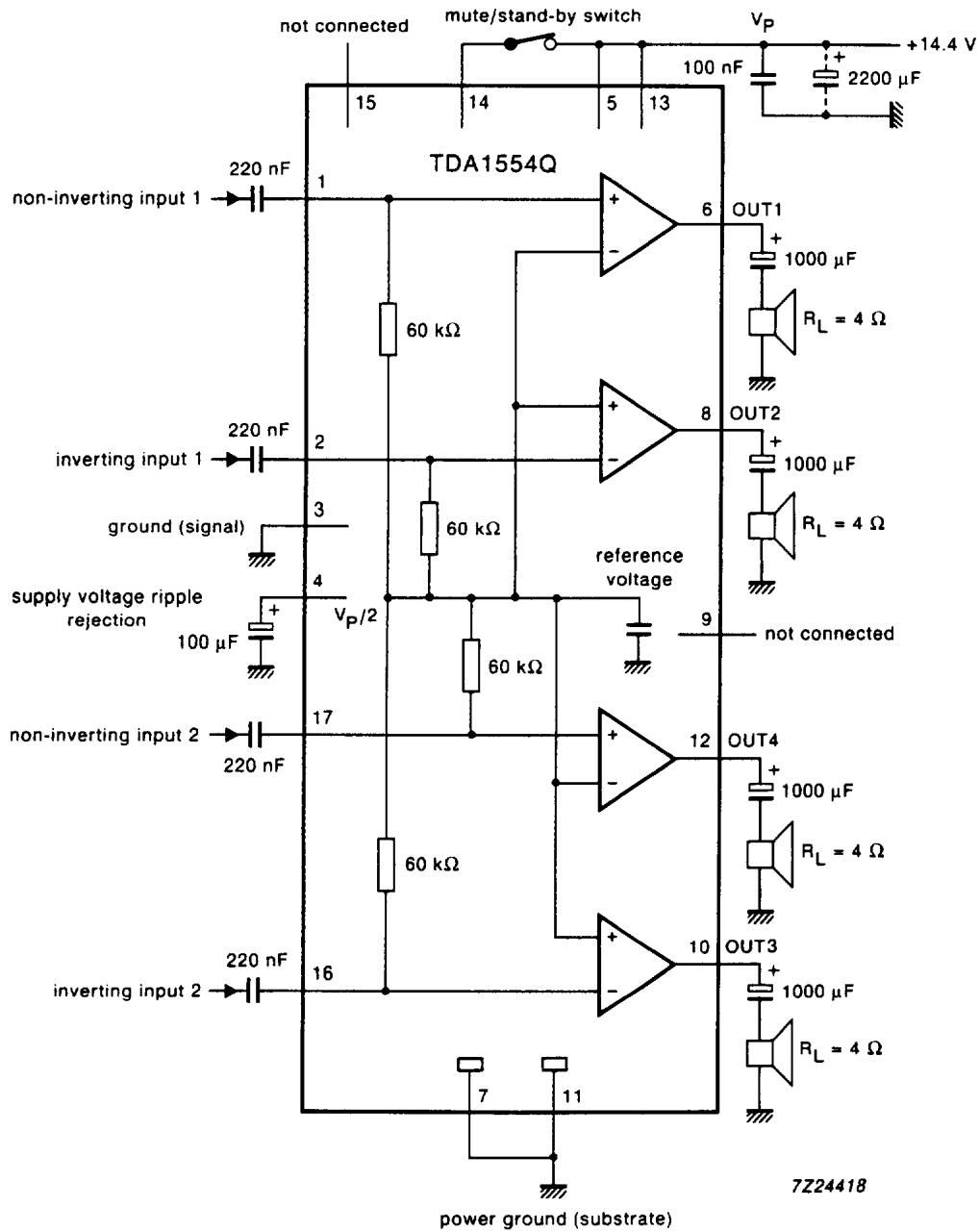


Fig.4 Quad single-ended application circuit diagram.

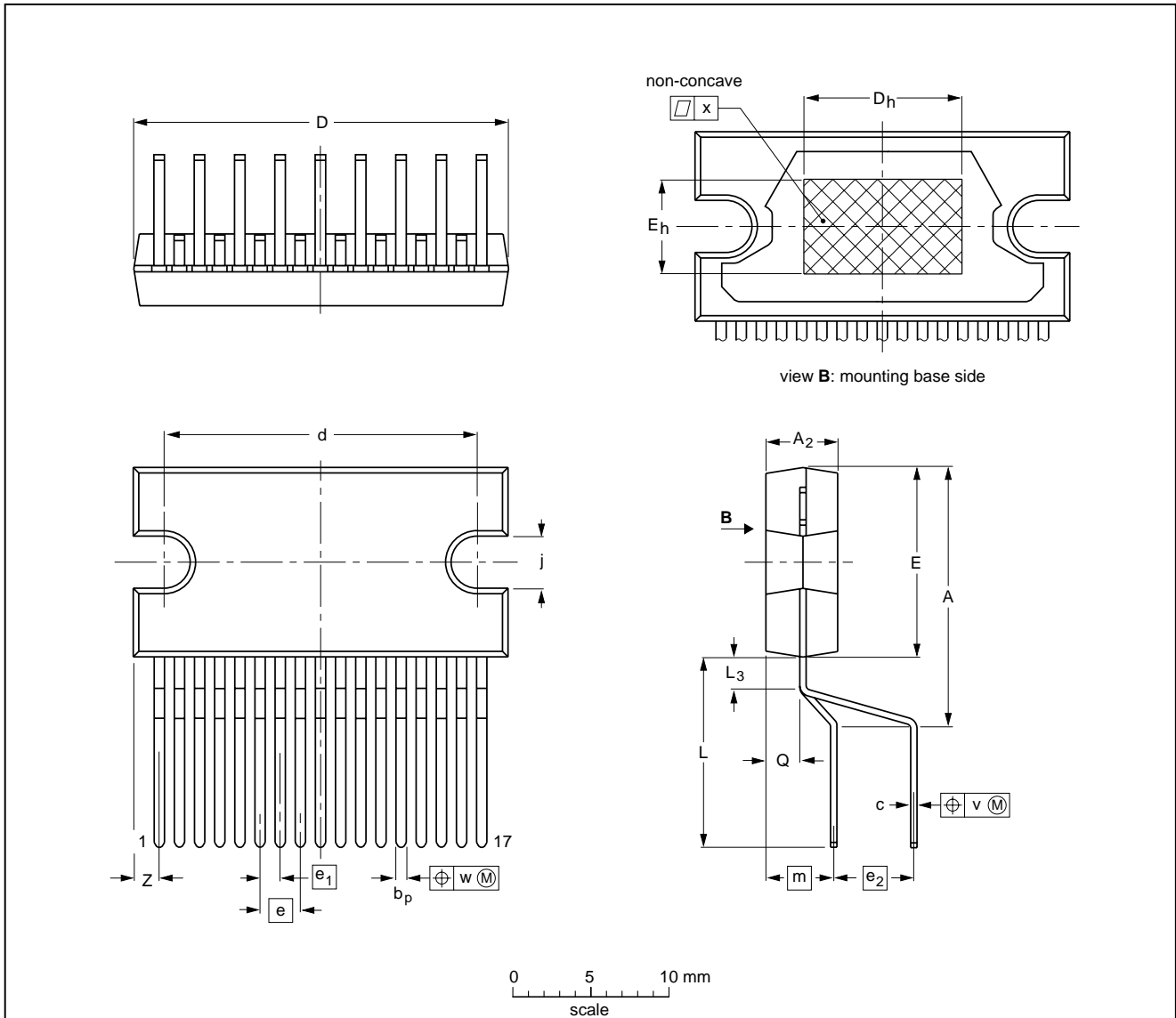
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						95-03-11 97-12-16

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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